# NANOELECTRONICS: APPLICATIONS AND ARCHITECTURES

**NRI-NRC Future Architectures Workshop- University of Notre Dame**

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**ONR Program Officer-Nanoelectronics (1973-2003)**

# THE NAVY APPROACH

**TO OBSERVE BUT NOT COMPETE WITH COMMERCIAL INDUSTRIES FOLLOWING-**

**“THE “ROAD MAP”**

**TO EXPLORE DIFFERENT MATERIALS, DIFFERENT DEVICES AND DIFFERENT ARCHITECTURES IN ORDER TO:**

**PROVIDE ADVANCED MILITARY SYSTEMS WITH CAPABILITIES IN COMPUTATIONAL SPEED, REDUCED ELECTRICAL POWER AND REDUCED COMPONENT VOLUME**

# BRIEF HISTORY

## “The Navy Nanoelectronics Program”

**1973- New Program Area**

**Radiation Effects in semiconductor devices**

**Contacts and interfaces between dissimilar materials**

**Shrinking silicon devices**

**=>Physics based modeling of semiconductor devices**

**1977- Major and Focused Program to Support Nanoelectronics Research**

**USER-Ultra Submicron Electronics Research**

**(NERD-Nano Electronics Research for Defense)**

**1997- ONR Grand Challenge program for Navy impact in 30-50 years**

**Multifunctional Electronics for Intelligent Naval Sensors**

# 1977-USER

**“Develop a long term basic research program leading to the development of electronics technology based on devices with 20 Angstrom dimensions” (2 Nanometers)**

## Major Components

**>Materials (thin film)**

Silicon

Compound semiconductors

Ferromagnetic films

**>Fabrication Technologies**

Electron Beam

Ion Beam

Patterned self-assembly

**>Device Physics**

Electronic-Magnetic-Optical

Nano- 3D, 2D, 1D, “0D”

Physics based device simulations

**>Computing Architectures**

Local interconnects

Parallel processing

3 Dimensional Integration

# 1997-ONR GRAND CHALLENGE
# "Multifunctional Electronics for Intelligent Naval Sensors"

***Research Programs To Impact on the Navy in 30 to 50 Years!***

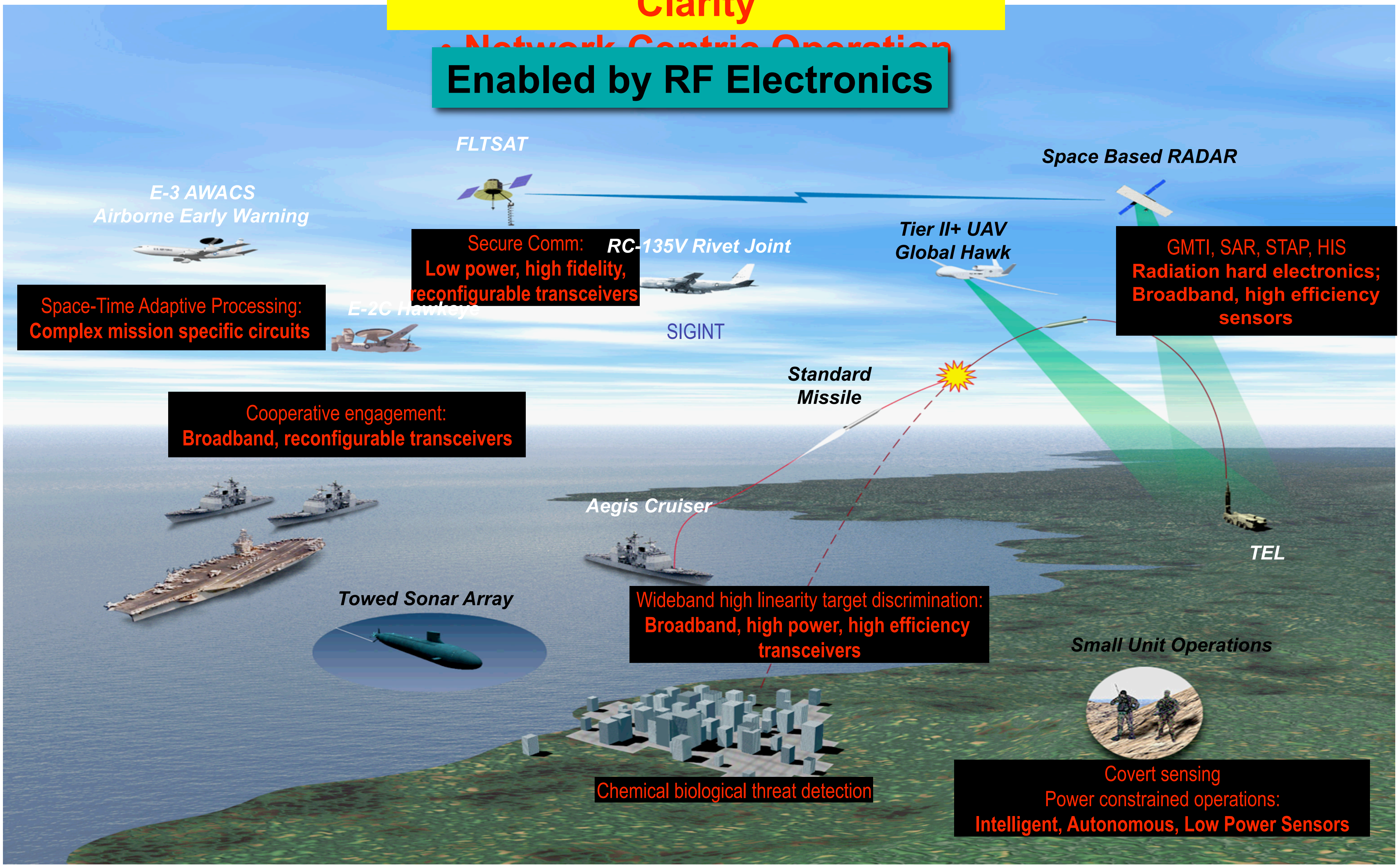
To develop highly multifunctional nanoscale devices to their **ultimate limits** of higher speed *(1000x),* lower power *(0.001x),* and smaller volume *(0.001x)* (SPV) and for systems that interactively combine sensing, image processing, computation, signal processing, and communications functions to achieve real-time adaptive response for Navy missions.

**NANOELECTRONICS IS THE KEY ENABLER**

# Asymmetric Advantage Enabled by *Information Superiority*

- **See Further with Greater Clarity**
- **Network Centric Operation**

**Enabled by RF Electronics**








# <u>FUTURE NAVAL CAPABILITIES</u>

- **Nanoelectronics will be a critical factor for FNCs**
  - <u>AUTONOMOUS OPERATIONS</u>
    - SENSOR DATA PROCESSING
    - INTELLIGENT_AUTONOMY
  - <u>ELECTRIC SHIPS</u>
    - INTELLIGENT SENSORS
  - <u>KNOWLEDGE SUPERIORITY & ASSURANCE</u>
    - IMAGE PROCESSING
    - INFORMATION MANAGEMENT
  - <u>MISSILE DEFENSE</u>
    - SMART WEAPONS SENSORS
  - <u>PLATFORM PROTECTION</u>
    - SMART WEAPONS SENSORS
    - DISTRIBUTED SENSORS
  - <u>TIME CRITICAL STRIKE</u>
    - DISTRIBUTED SMART SENSORS
    - IMAGE & VIDEO ANALYSIS
  - <u>WARFIGHTER PROTECTION</u>
    - SIGNIFICANTLY ENHANCED SITUATION AWARENESS
      (automatic response)

# "Finding the Right Device for the Application"
# NANOELECTRONIC DEVICES

**NOW**

- SILICON TRANSISTORS
- NANOMAGNETIC DEVICES
- HETEROJUNCTION DEVICES
- RESONANT TUNNELING DEVICES
- PROGRAMMABLE METALLIZATION CELL MEMORY (PMC)

**NEXT?**

- SINGLE ELECTRON DEVICES
- SPINTRONIC DEVICES
- NANOMAGNETS FOR MQCA
- CARBON NANOTUBES
- SPIN TORQUE MEMORY (DARPA)
- SCHOTTKY GATE SUBTHRESHOLD TRANSISTORS

**NEVER?**

- MOLECULAR TRANSISTORS
- NANOWIRE TRANSISTORS
- RESONANT TUNNELING TRANSISTORS
- MAGNETIC RTD
- QUANTUM COHERENT TRANSISTORS
- GRAPHENE TRANSISTORS
- DOMAIN WALL MEMORY/LOGIC
- NANO MEMRISTOR
- NANO MEMINDUCTOR
- NANO MEMCAPACITOR

# INFLUENCING/DOMINATING FACTORS

**SPEED-Terahertz Digital Signal Processing**

**AMRFS-Advanced Multifunctional RF Systems**

**POWER-Non-Volatile Reprogrammable Computing**

**Legacy electronics**

**Hybernating or "instant-turn-on-computing"**

**Low dissipation power**

**VOLUME-High performance hybrid integrated systems (SoC)**

**Surveillance**

**Targeting and tracking**

**Bio-inspired Neuro-Computing**

# SPEED

**Compound Semiconductors**

- **High Mobility**
- **Low voltage**
- **Flexibility in hybrid systems**
- **6.1 Angstrom- InAs/AlSb/GaSb (Lattice matched)**

**InGaAs/InP**

**GaAs/GaAlAs**

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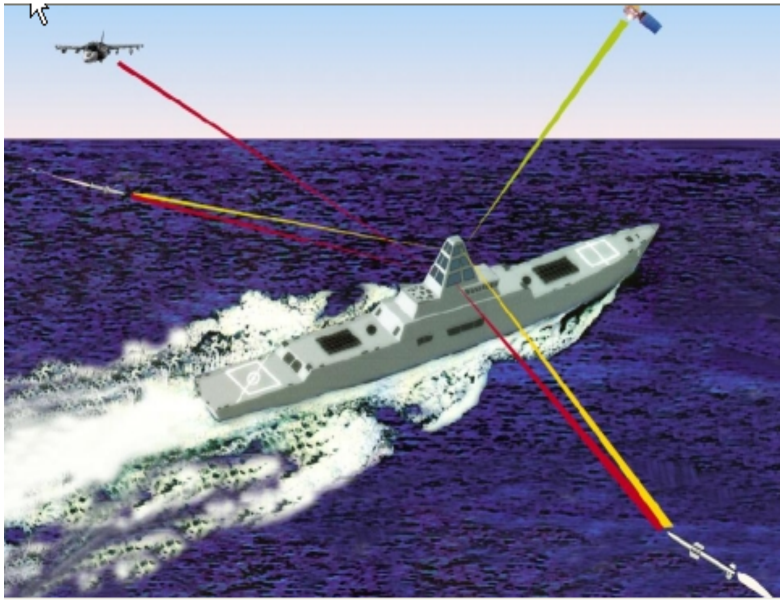
**HFETs**

**Resonant Tunneling Diodes [f(T) > 3 THz]**

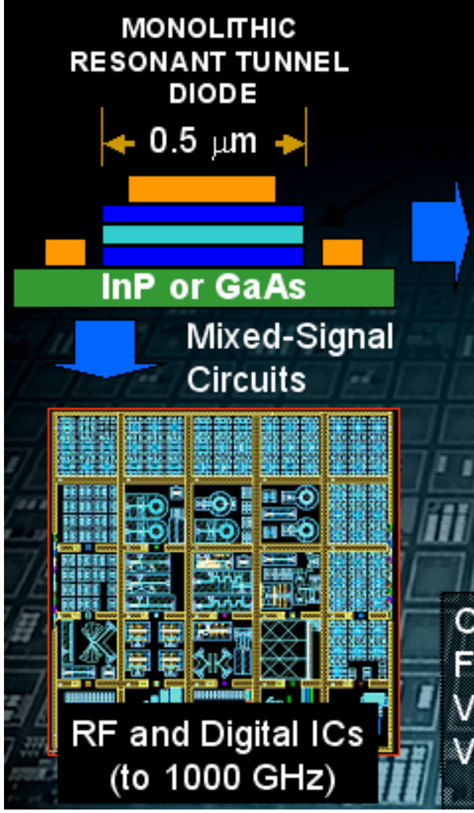
**Advanced *Multifunction* RF-Concept (AMRF-C)-Cellular Antenna Arrays**

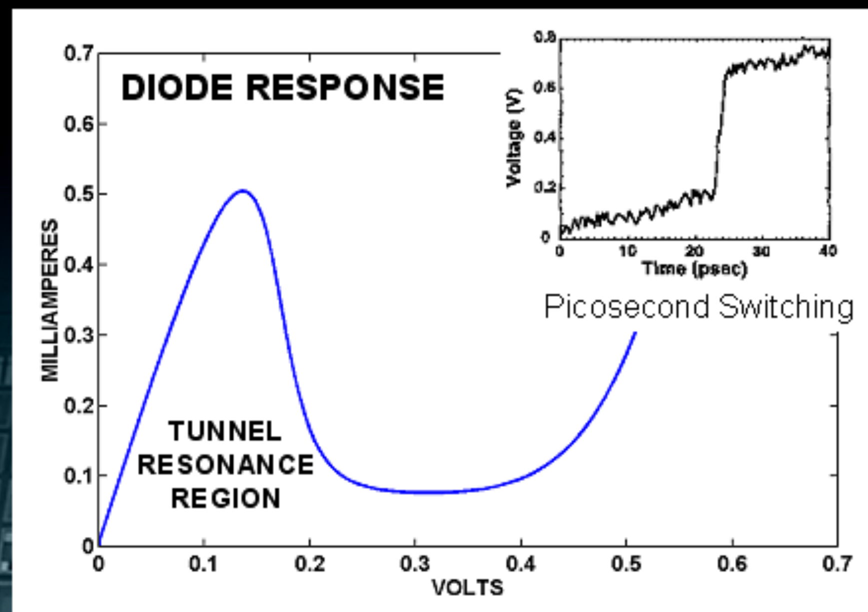
**Wideband (10-100 GigaHertz) *Digital* Antennae for Digital Beam Forming**

- **Radar**
- **Communications**
- **Electronic Warfare**
- **SAR-Synthetic Aperture Radar**

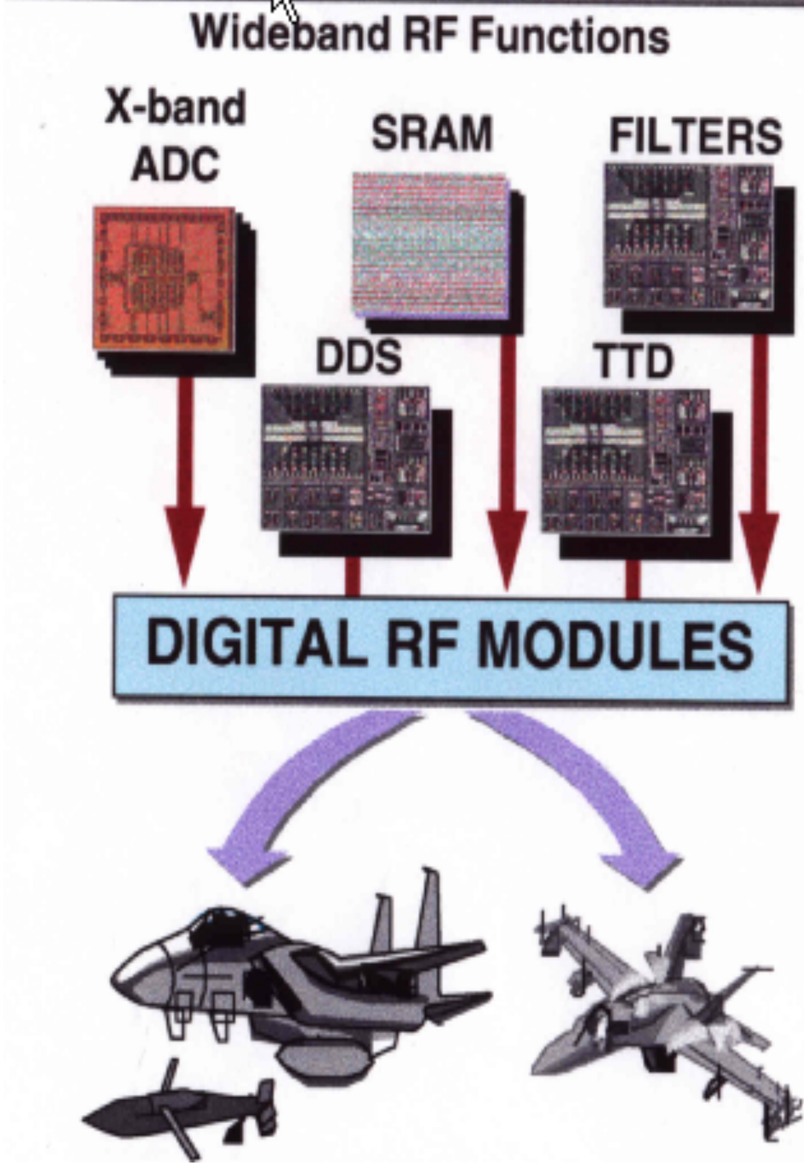
**(Colleague question-can we make 400 GigaHertz DSPs?)**

# Resonant Tunneling Basics




Cut-off frequency ~ 1000 GHz in standard devices
$F_{cut\text{-}off}$ can be > 3000 GHz in optimized Sb-based RTDs
Very sensitive and stable quantizer for A/D, D/A, Logic
Very Rad Hard and Temperature stable (NRL)



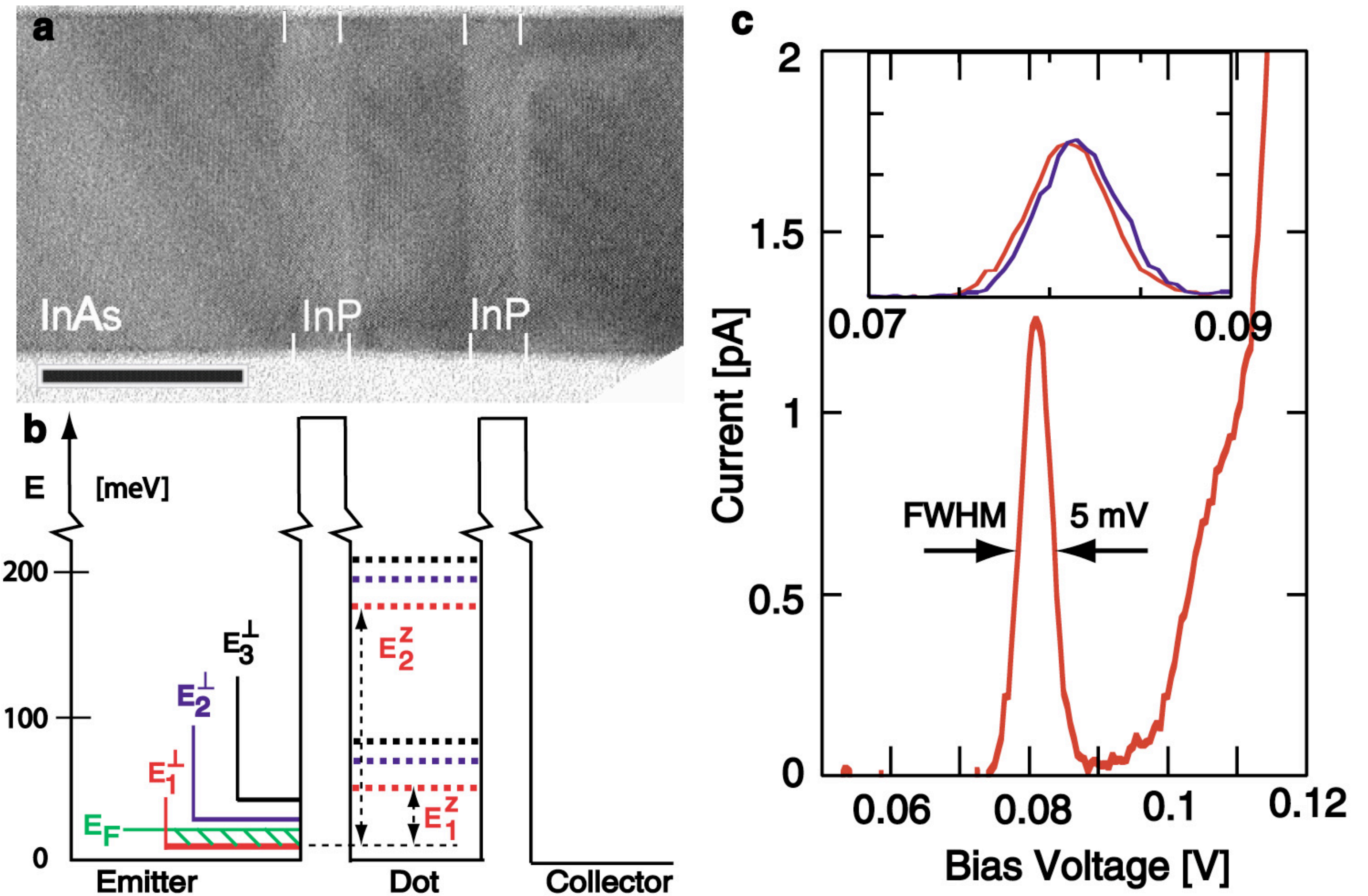

## PROJECT OBJECTIVE:

- Provide 10-100 GHz mixed signal components for advanced digital RF systems
- **FEATURES:**
  - Production InP IC Process
  - Resonant Tunneling Devices
  - FET/HBT Compatibility

## DoD BENEFITS:

- Component base for wideband digital RF Systems - Radar, SAR, Comm, RWR, EW
- 10-100 GHz ADC / DAC / DDS / Logic
  - 4-10 GHz Digital IF
  - Digital X-band Phased Arrays
- 1000X Lower power microwave SRAM
  - True Time Delay / FIFOs / Buffers

First implementation of a 1D heterostructure nanoelectronic device in as a double-barrier resonant tunneling diode (DBRTD) in InAs with InP b



# POWER

**Nano Magnetics**

- Non-volatile Memory/Logic
- Dilute magnetic semiconductors (Spintronics)
- Hybrid magnetic/semiconductor (magnetic state variable?)

**High mobility semiconductors (HFETs and RTDs)**

- Low voltage
- High Speed
- Fewer devices per function

**Non-volatile Memory**

**NON-VOLATILE**

**ELECTRONICS**

**Nano-magnetics**

- **Programmable/Reprogrammable Logic**
  - **Universal Circuits (?)**
- **Battery life**
- **Radiation Hard**
- **Legacy Electronics**
- **Instant-turn-on-computer**

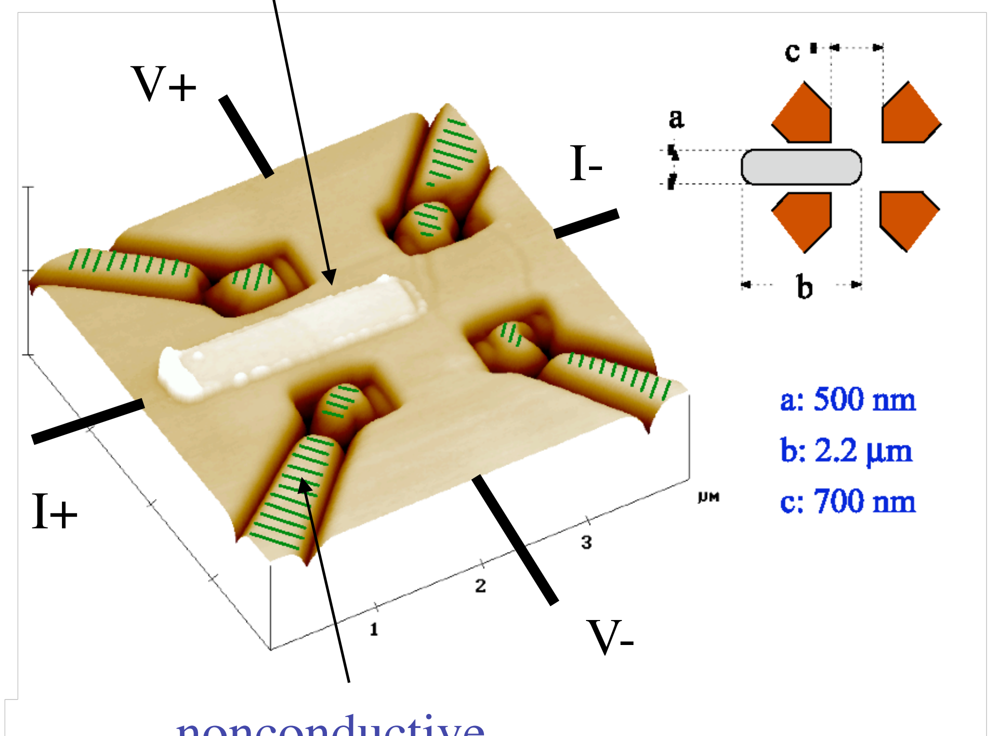
# Magnetoelectronic Reprogrammable Logic

- New paradigm for **Programmable** (and **Reprogrammable**) **Logic**
- Reduce dependence on ASIC components.
- Low cost, multifunctional alternative:
  - **Reprogram by software** (data input stream) - hardware upgrade (reprogram chip function) can be achieved by software; **fast and inexpensive;** test and reprogram to achieve self-healing circuits
  - Rad hard; multi-GHz operation
  - **Dual-use** applications, such as satellite (and other space based systems), missile guidance units, consumer electronics, etc.
- Inexpensive alternative: Field Programmable Gate Arrays (FPGA)
  - Single design: array of identical blocks, each with “programmable” function

# HHE-Hybrid Hall Effect Device
# (Research Prototype-sub-micron)

Ferromagnetic element

**AFM image**

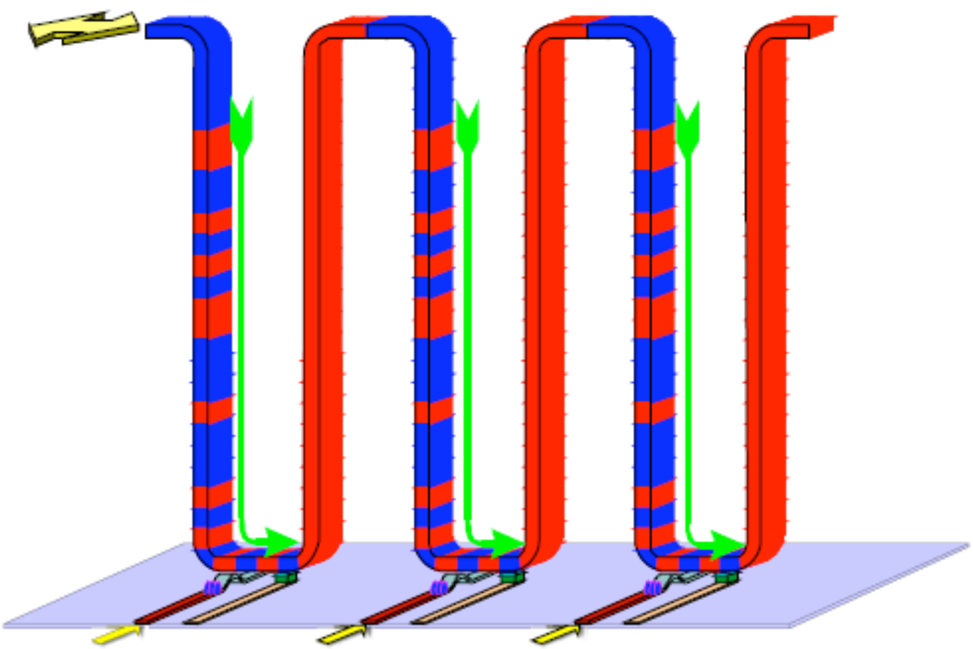



nonconductive region; radiation damage by FIB

- **Demonstrate scaling to f = 500 nm**
- Single F layer - 500 nm by 2.2 µm, 55 nm thick $Ni_{0.8}Fe_{0.2}$
- mobility of S: 4500
- 30 mV output level

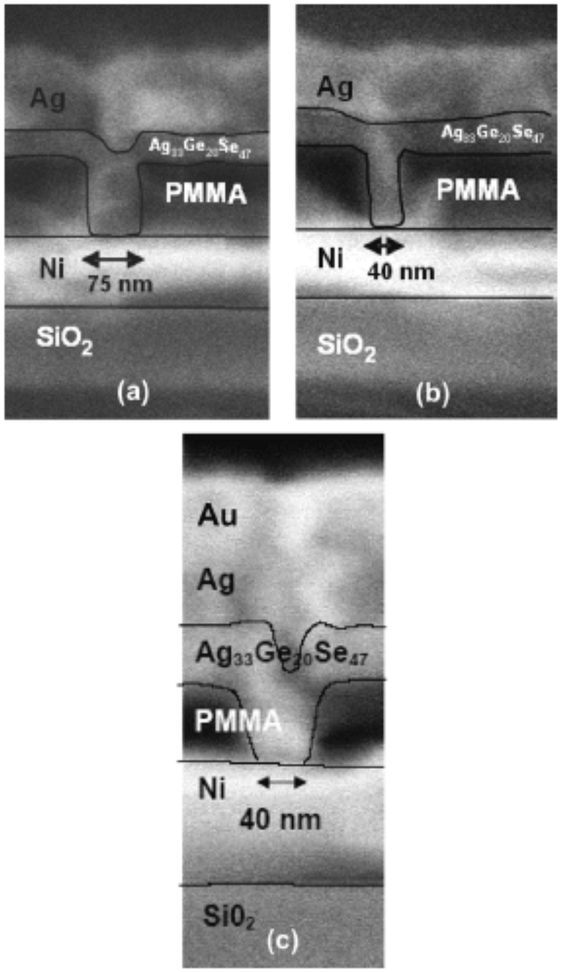
Mark Johnson, NRL

## Magnetic Shift Register Memory



→Magnetic race-tracks can be connected in series
→Many other configurations possible

# <u>NON-VOLATILE</u> PROGRAMMABLE METALLIZATION CELL (PMC)



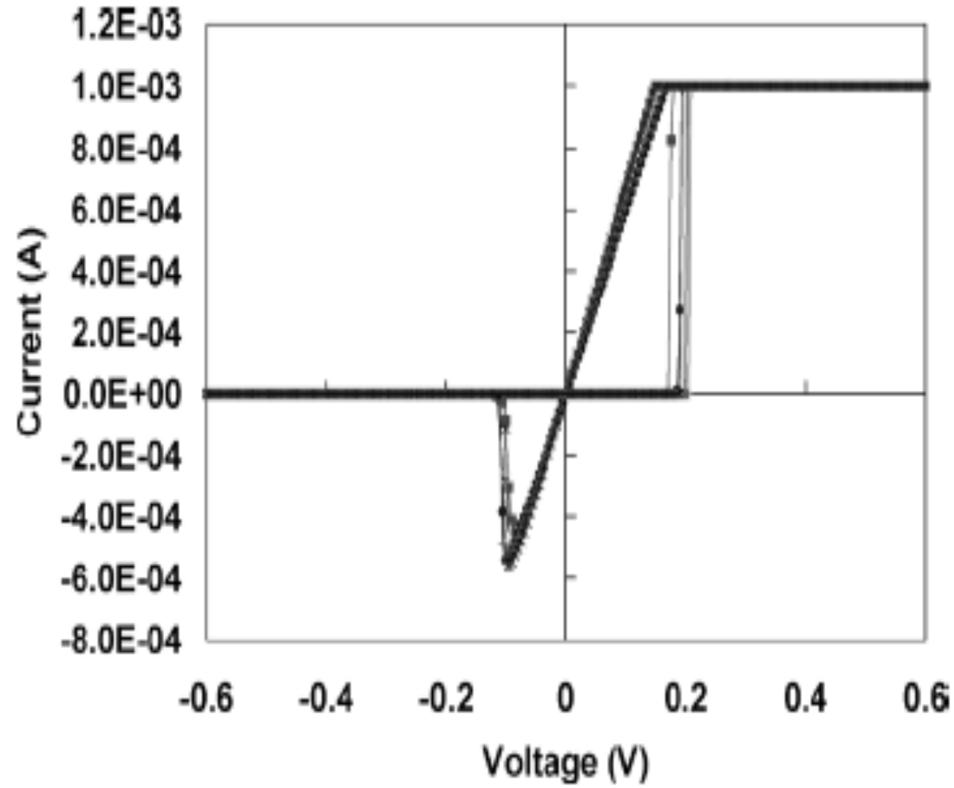




Fig. 4. Current–voltage plot from a 40-nm structure fabricated using process B obtained using six voltage sweeps of −0.6 to +0.6 to −0.6 V with a 1-mA current limit. The device switches from over $10^7\ \Omega$ to its low resistance state of $100\ \Omega$ around 0.2 V and the conducting pathway breaks at −0.1 V.

# Programmable Metallization Cell Memory Performance Summary

- Low voltage → <0.5 V
- Low current → typ. 10 μA (to 10 nA)
- Low power → μW (to nW)
- High speed → <20 ns write/erase/access
- Low energy → pJ to fJ operation
- High retention → >10 years at elevated T
- High endurance → >>$10^{12}$ cycles
- High off/on ratio → >$10^{5}$
- Good scalability → <10 nm
- Analog $R_{on}$ → GΩ to tens of Ω programmable
- MLC capability → 2 bits per cell shown, >2 possible
- High density → Tb/chip possible at 22 nm with MLC
- Integrable → 1 mask over logic, **BEOL compliant**
- Low cost → DRAM-like projections

# VOLUME

**Digital functions**

**Analog functions**

**Embedded memory**

**3 Dimensional integration**

# NANO-ARCHITECTURES?

CROSS-BAR

CMOL

QCA/MQCA (field coupled devices)

MOLECULAR (directed self-assembly)

PIP (Propagated Instruction Processor)

3 DIMENSIONALLY INTERCONNECTED PROCESSORS

NEURO-INSPIRED

CELLULAR AUTOMATA

SPIN BASED RECONFIGURABLE LOGIC

ARTIFICIAL NEURAL NETWORKS

CELLULAR NONLINEAR NETWORKS/CELLULAR NEURAL NETWORKS

“CNN-UNIVERSAL MACHINE”

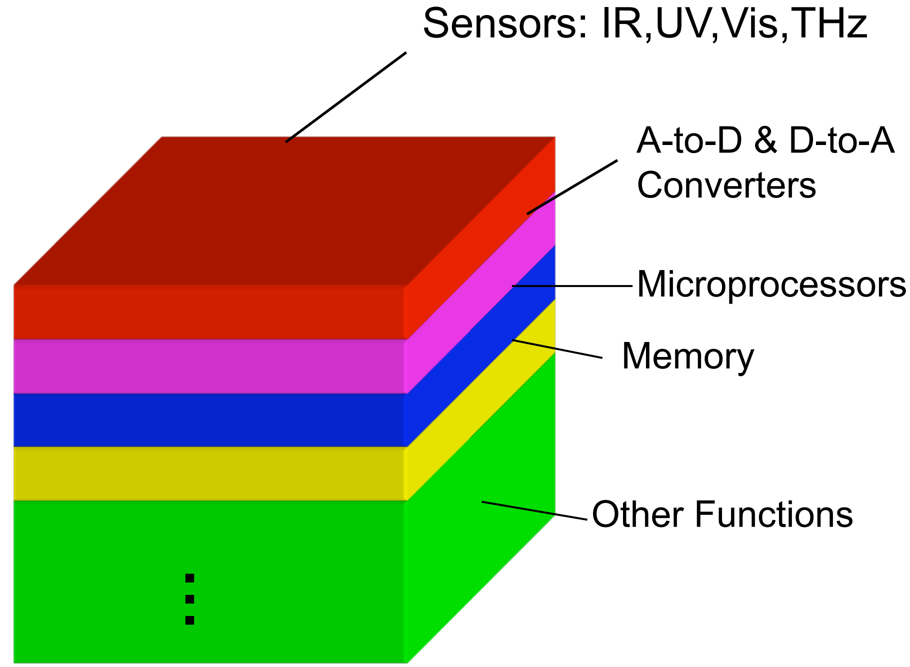
# 1998-GRAND CHALLENGE
## “Multifunctional Electronics for Intelligent Naval Sensors”
(To impact on the Navy in 30-50 years!)

Three-dimensional, ultra-dense, stacks of layers, each with a different function, ranging from sensors, to analog-to-digital converters, microprocessors, and memories.

Devices in each layer featuring sub-10 nm dimensions and low-power-consumption, and often operating on non-classical phenomena such as quantum, or spin, or single-electron effects.

Layers intelligently connected with each other i.e. vias or nanowires.

Other Functions:
- adaptive control
- optical communication
- energy harvesting




**Speed-1000X**
**Power-1000X**
**Volume-1000X**

# SOLUTION

## CNN-UNIVERSAL MACHINE

LOCAL INTERCONNECTS

PARALLEL COMPUTING

NO CLOCK SKEW PROBLEMS

NO WIRE DELAY PROBLEMS

NO WIRE-TO-WIRE COUPLING

ANALOG OR DIGITAL DEVICES

PROGRAMMABLE FUNCTIONS

INTEGRATED MEMORY

MULTIFUNCTION INTEGRATION

MULTIPLE LAYERS (INTERCONNECTED)

## NANOSCALE?

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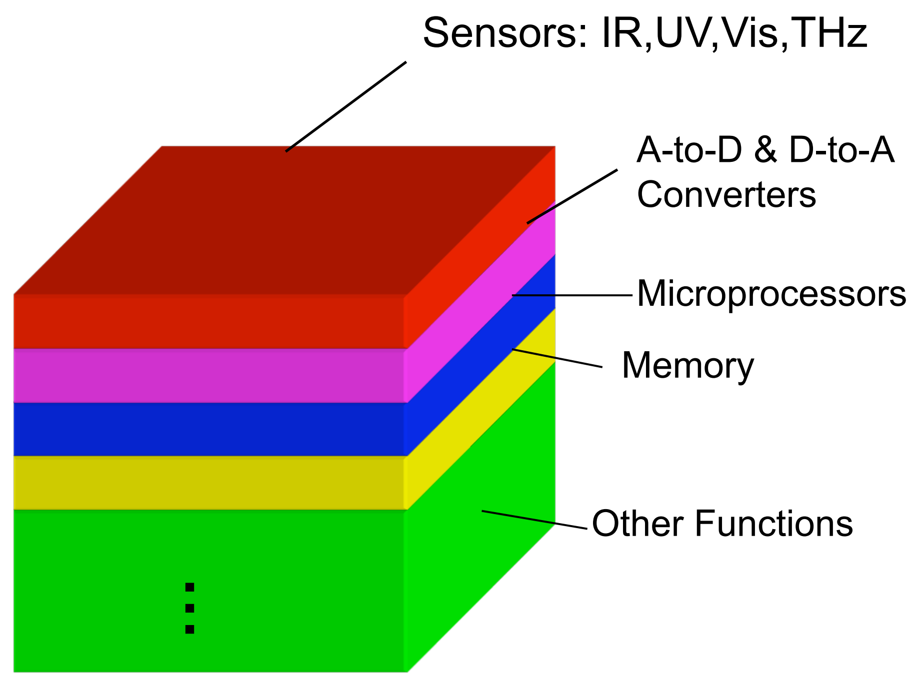
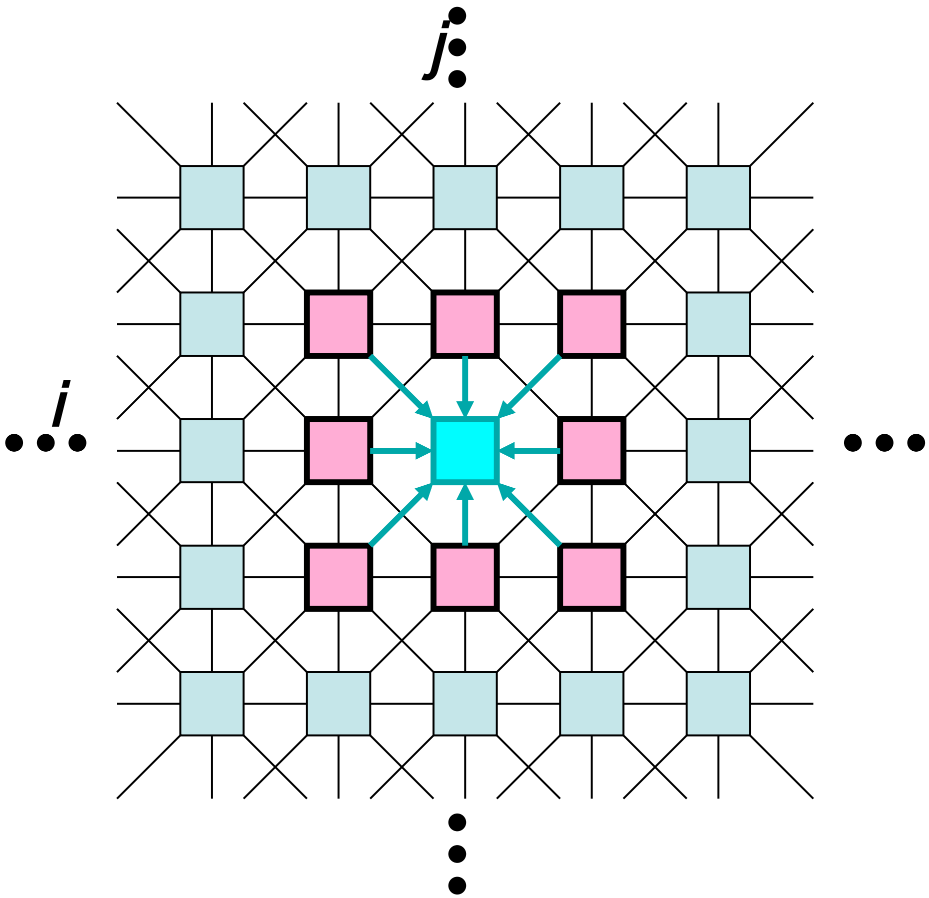



**Speed-1000X**
**Power-1000X**
**Volume-1000X**

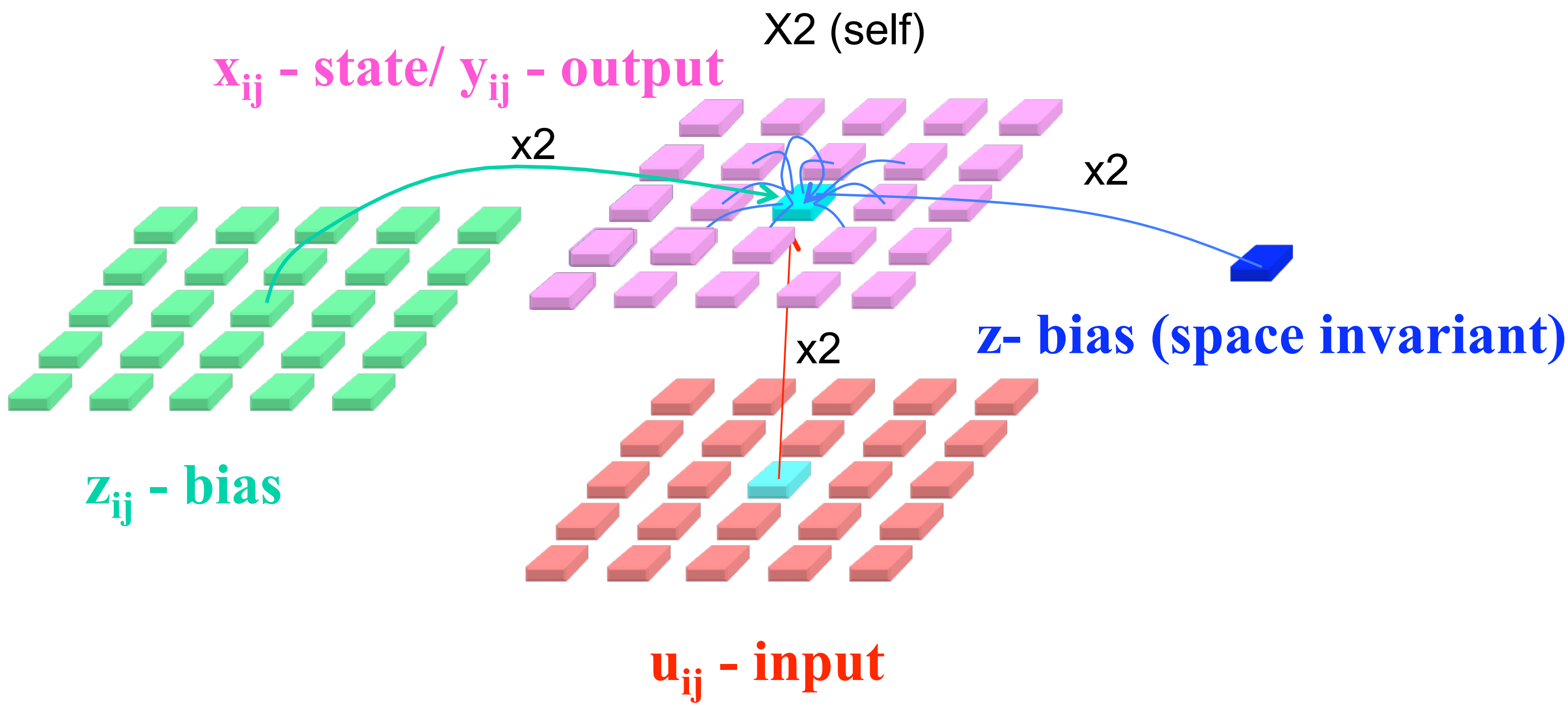
# Introduction to CNN Dynamics




The **Cellular Nonlinear/Neural Network** (CNN) is:

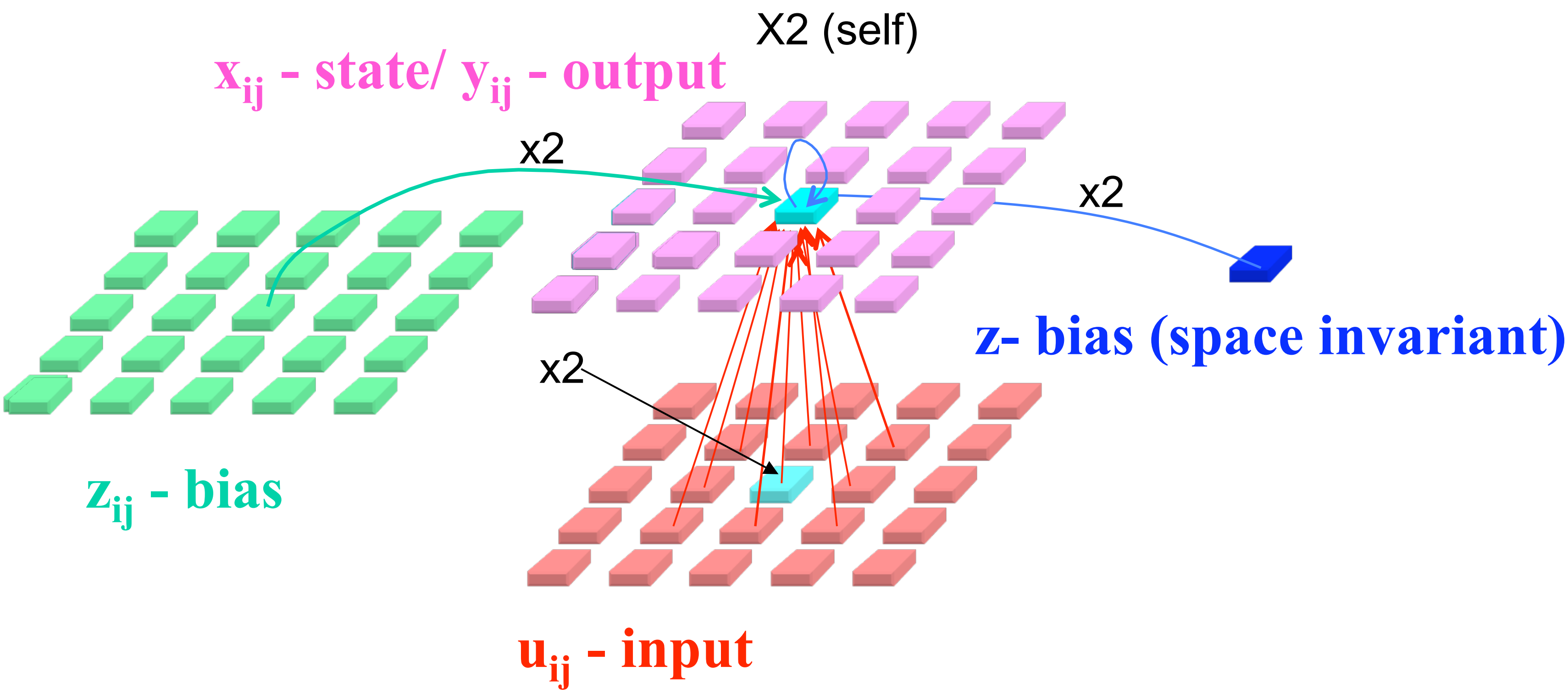
- an **analog** processor array
- on a 2D grid
- with mainly local interactions.

# Template configurations I: Spatial feedback




$$\mathbf{A} = \begin{bmatrix} a_{-1-1} & a_{-10} & a_{-11} \\ a_{0-1} & a_{00} & a_{01} \\ a_{1-1} & a_{10} & a_{11} \end{bmatrix}, \qquad \mathbf{B} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & b_{00} & 0 \\ 0 & 0 & 0 \end{bmatrix}, \qquad z_1 = i_0, \quad z_{ij} = i_{ij}.$$

# Template configurations II: Spatial feed-forward




$$\mathbf{A} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & a_{00} & 0 \\ 0 & 0 & 0 \end{bmatrix}, \quad \mathbf{B} = \begin{bmatrix} b_{-1-1} & b_{-10} & b_{-11} \\ b_{0-1} & b_{00} & b_{01} \\ b_{1-1} & b_{10} & b_{11} \end{bmatrix}, \quad z_1 = i_0, \quad z_{ij} = i_{ij}.$$

**Name:** **THRESHOLD CNN**

**Task Prescription:** *Convert a gray-scale image* P *(loaded as initial state) into a binary image where each pixel* $p_{ij} \in$ P *is converted into "black" ("red" in pseudo-color) if, and only if,* $p_{ij}$ *has a gray scale intensity exceeding a prescribed value equal to the CNN threshold* $z^*$. *In the two extreme cases when* $z^*=1$ *and* $z^*=-1$ *all output pixels will be printed in black (red), or in white (blue) respectively.*

## *Cloning Template*

$$z: \boxed{z^*} \qquad \mathbf{B}: \begin{array}{|c|c|c|} \hline 0 & 0 & 0 \\ \hline 0 & 0 & 0 \\ \hline 0 & 0 & 0 \\ \hline \end{array} \qquad \mathbf{A}: \begin{array}{|c|c|c|} \hline 0 & 0 & 0 \\ \hline 0 & 2 & 0 \\ \hline 0 & 0 & 0 \\ \hline \end{array}$$

## *Boundary Condition*

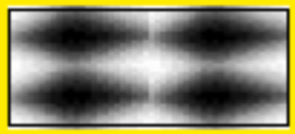
*Fixed:* $x_{i^*j^*}=0, \quad u_{i^*j^*}=0$

*($i^*j^*$ denotes boundary cells)*

## *Initial State*

$x_{ij}(0)$ *= a given gray-scale image*

**Example 1:** Array Size = 30 x 48; $z^*= -0.5$



*Input Image: arbitrary* *Initial State* *Output Image*

**Example 2:** Array Size = 256 x 320; $z^*= -0.5$

| Name: | **CONTOUR EXTRACTION CNN** |
|---|---|
| **Task Prescription:** | *Extract contours which resemble edges (resulting from big changes in gray level intensities) from gray-scale images.* |

Gene

G

| | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0.7 | a | a | a | a | 0 | a | a | a | a | 0 | 0 | 0 | 0 | 2 | 0 | 0 | 0 | 0 |

$$a = 0.5\,[\,\mathrm{sgn}(u_{ij} - u_{kl} - 0.18) - \mathrm{sgn}(u_{ij} - u_{kl} + 0.18) + 1\,]$$

*Boundary Condition*

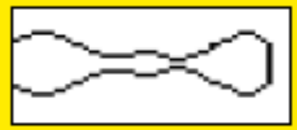
*Fixed:* $x_{i^*j^*} = 0, \quad u_{i^*j^*} = 0$

*($i^*j^*$ denotes boundary cells)*

*Initial State*

$x_{ij}(0) = u_{ij} =$ *input image*

**Example 1: Array Size = 30 x 48**



*Input Image* | *Initial State* | *Output Image*

**Example 2: Array Size = 256 x 256**

# SAMPLES OF CNN TEMPLATES (GENES)

**CONTOUR EXTRACTION**

**CORNER DETECTION**

**HORIZONTAL TRANSLATION**

**VERTICAL TRANSLATION**

**DIAGONAL TRANSLATION**

**POINT EXTRACTION**

**THRESHOLDING**

**DEBLURRING**

**EROSION**

**HALF TONING**

**GRADIENT DETECTION**

**MANY MORE**

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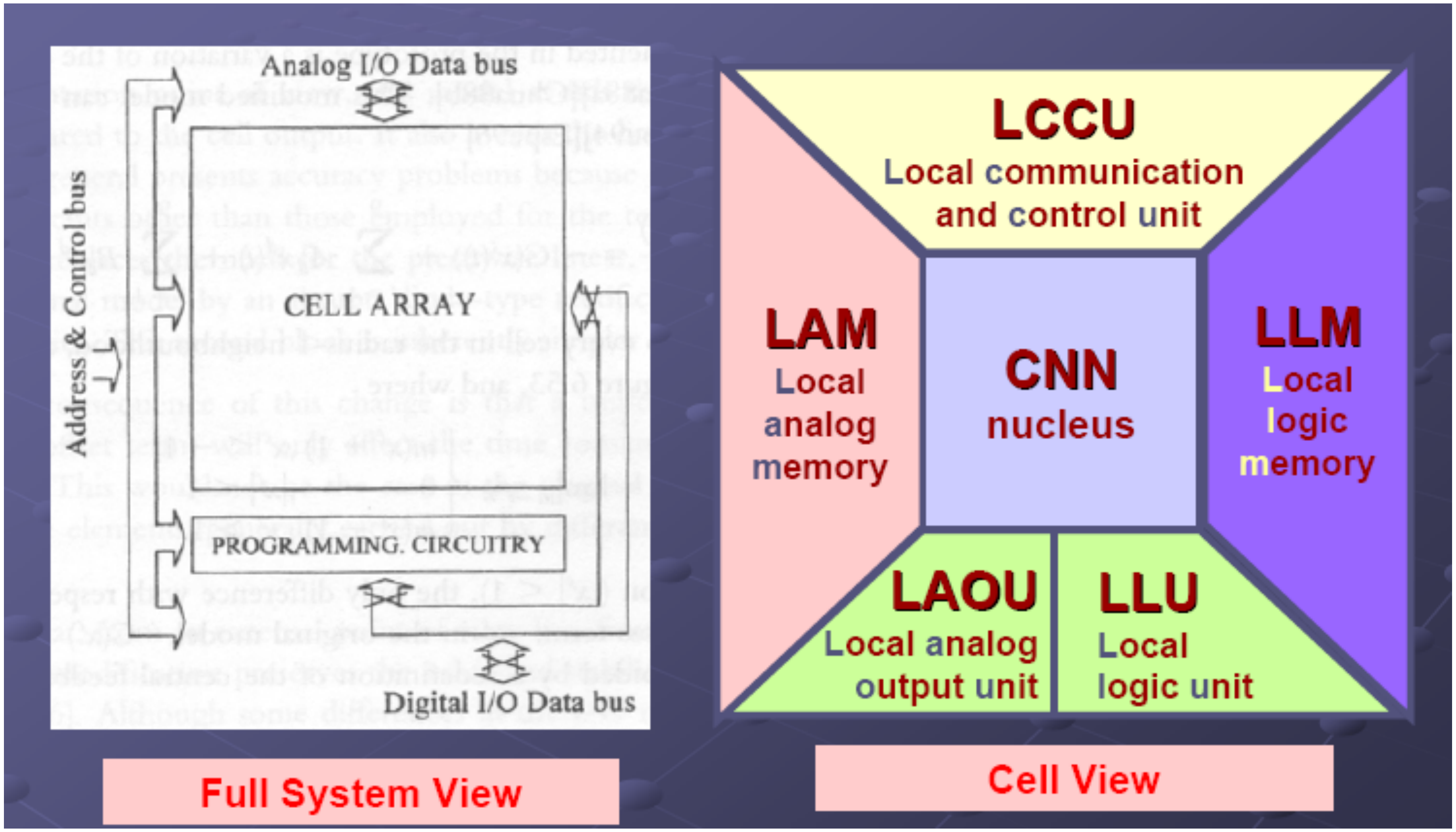
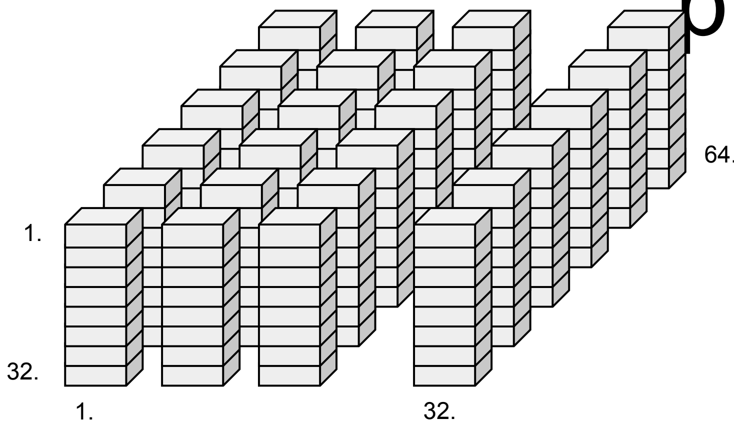
**Image processing or pattern recognition involves using the programming language to run an algorithm using one or more of the templates. One template run can take 1 microsecond.**




**INTEGRATE DETECTOR WITHIN THE CELL OR THROUGH BUS CONNECTIONS**

# Comparison between an IBM Cellular Supercomputer and an analogic processor



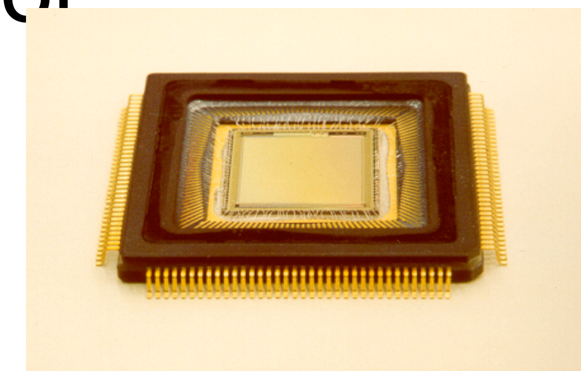

**65536 (32*32*64) Power PC**

***IBM Cellular Supercomputer 2002***

Computing Power ~ 12 * $10^{12}$ (**TeraFLOPS**)

A = 65536 x 1.06 $cm^2$ = **6.9468 $m^2$**

P = **491 kW**



128 x 128 processor with optical input

***An analog-and-logic CNN supercomputer***

Computing Power ~ 12 * $10^{12}$ (**TeraOPS**) equivalent

A = **1.4 $cm^2$**

P = **4.5 W**

# UNIQUE FEATURES OF CNN-UM IMAGE PROCESSING

FULLY PROGRAMMABLE IMAGE PROCESSING COMPUTER ON A SINGLE CHIP

POWER DISSIPATION ORDERS OF MAGNITUDE SMALLER THAN WITH DIGITAL PROCESSORS

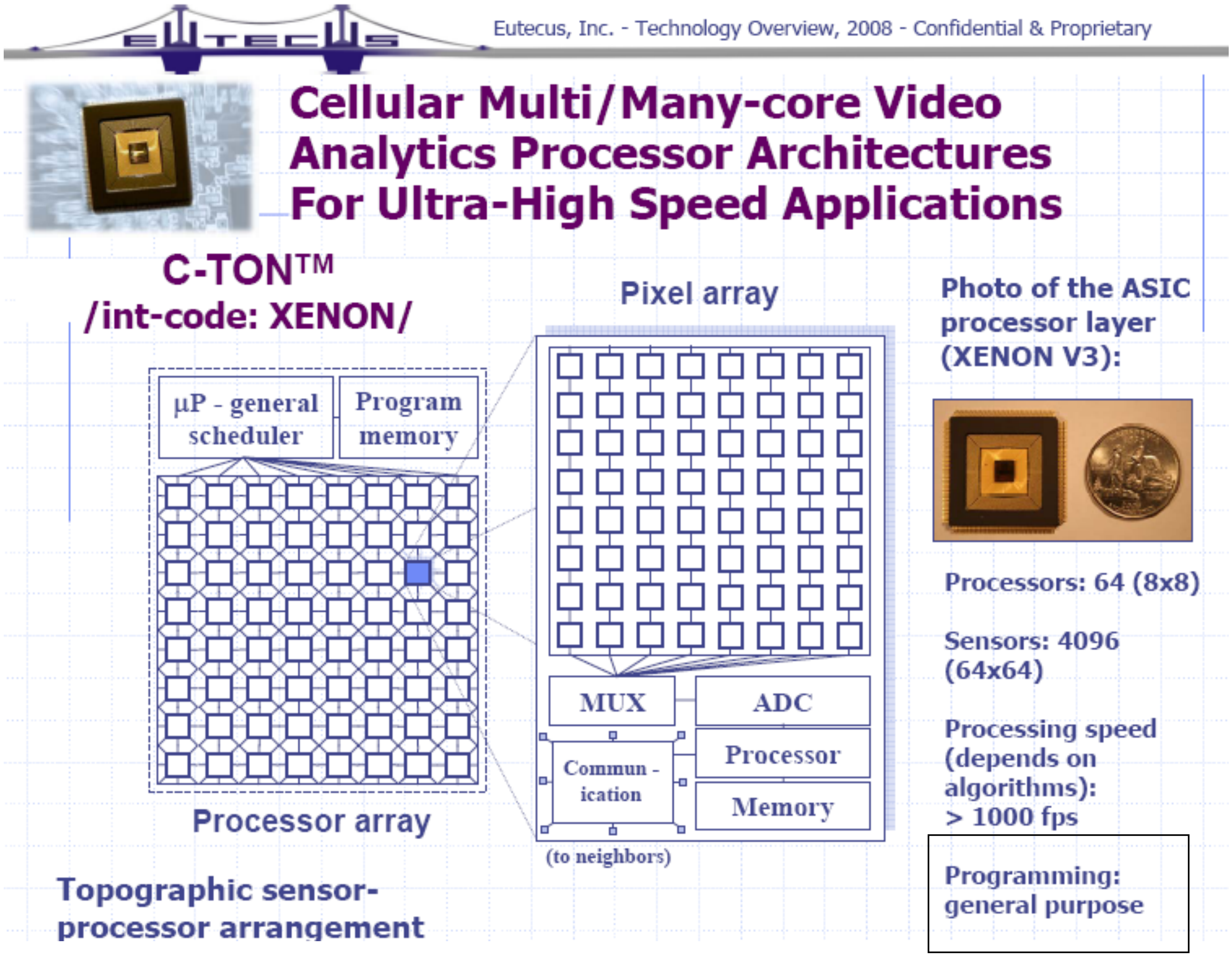
INTEGRATES PHOTODETECTOR SIGNALS DIRECTLY ONTO PROCESSOR CELLS

HIGH LEVEL PROGRAMMING LANGUAGE FOR ADAPTING TO ANY DESIRED IMAGE PROCESSING ALGORITHM

IMAGE INPUTS CAN BE DIGITAL OR ANALOG (ON-CHIP ADC AND DAC)

HIGH FRAME RATES SIGNIFICANTLY LARGER THAN DIGITAL PROCESSING

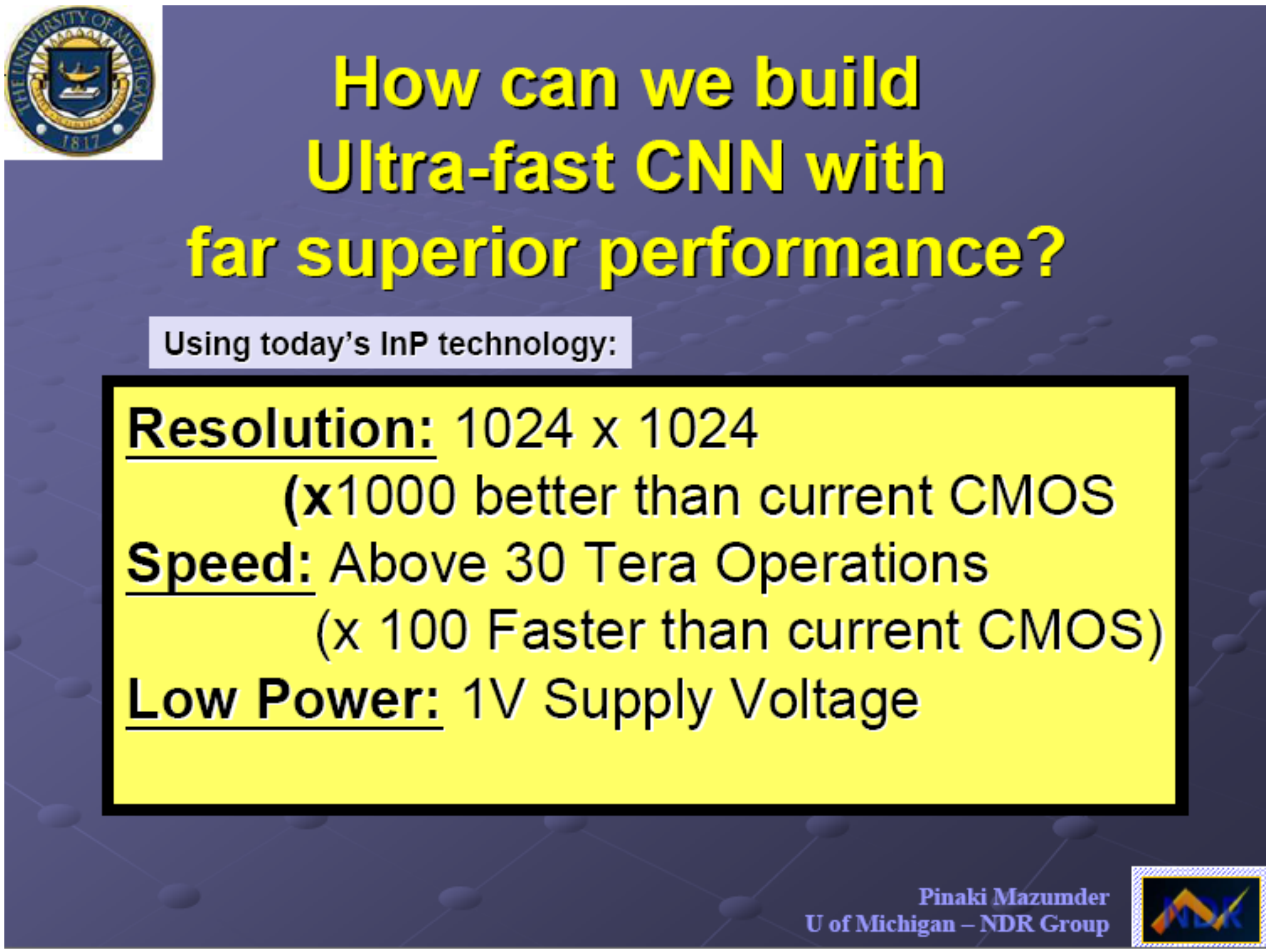
CELL FUNCTION IS EITHER ANALOG OR DIGITAL




45 nanometer silicon technology

## RTD BASED CNN CIRCUIT SIMULATION (2003)

### Pinaki Mazumder (U Michigan)



## <u>SAMPLE LIST OF APPLICATIONS:</u>

AUTOMATIC TARGET RECOGNITION – ATR

UAV & MAV FOR SURVEILLANCE (BORDER?)

AUTONOMOUS VEHICLE NAVIGATION WALKING/CLIMBING ROBOTS

MULTIPLE TARGETS (TARGETING AND TRACKING)

MONITORING STREAMING VIDEO DATA (ON-SITE PROCESSING)

FACIAL RECOGNITION

HYPER-SPECTRAL SURVEILLANCE AND INTRUDER IDENTIFICATION

COLLISION AVOIDANCE

TRAFFIC CONTROL CAMERAS (!)

TACTILE SENSORS FOR ROBOTS (3 Dimensional)

SOUND LOCATOR

TOYS/GAMES

NEURO INSPIRED COMPUTING-<u>"ARTIFICIAL EYE"</u>

# NEUROMORPHIC ENGINEERING

Bionics-implanted devices with hybrid digital-analog computing

Bionic ear (cochlear)

Bionic eye (retina)

Monitoring brain functions (control of epileptic seizures)

Wireless

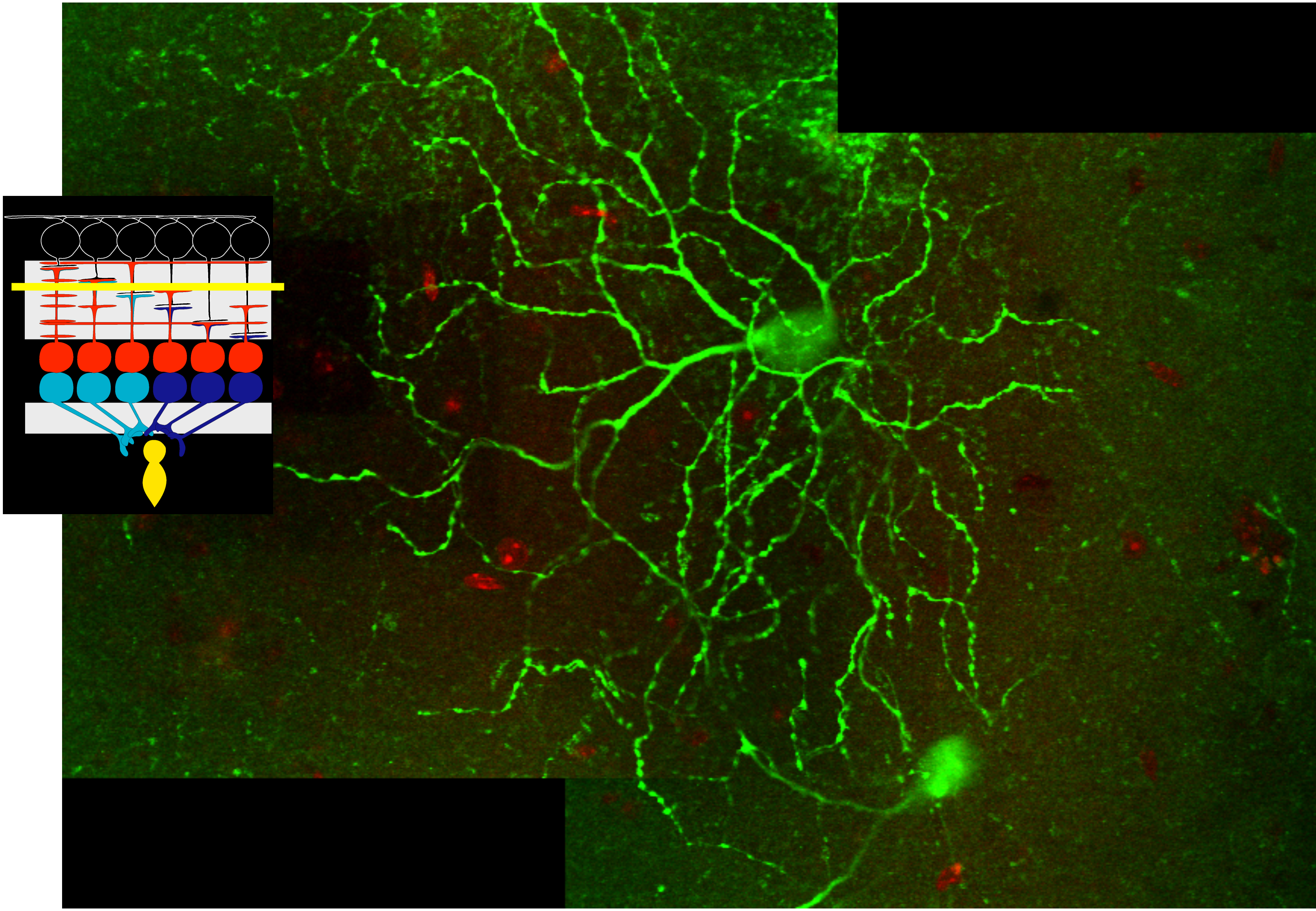
Nano-power (Low power battery with wireless recharging)

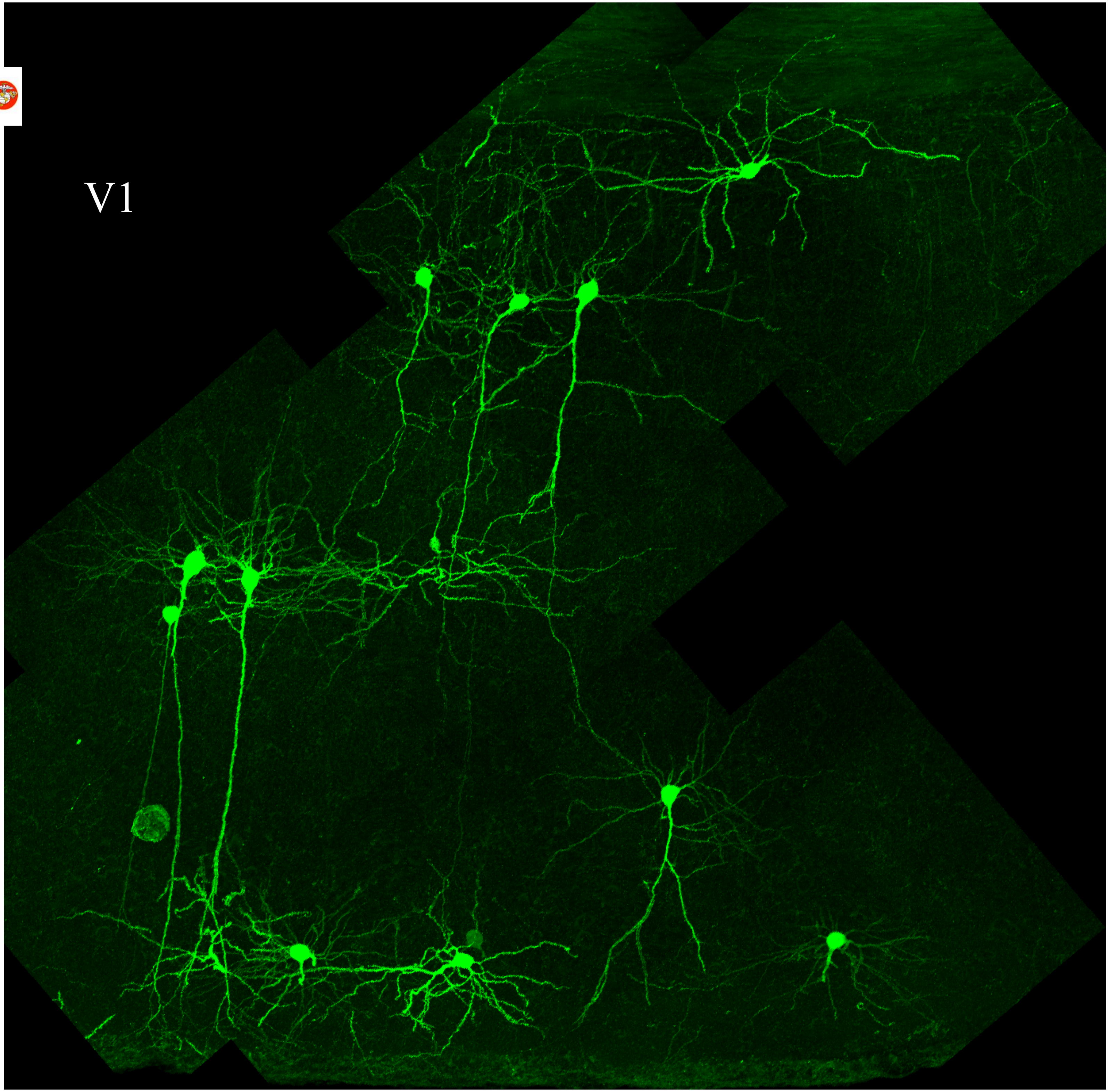
Material compatibility

Energy harvesting

Largest Obstacles:

- Connection to neuronal networks
- Determining and replicating cortical neuronal networks
- Analysis of action potentials of neuronal systems

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# NANOELECTRONICS AND NEW ARCHITECTURES

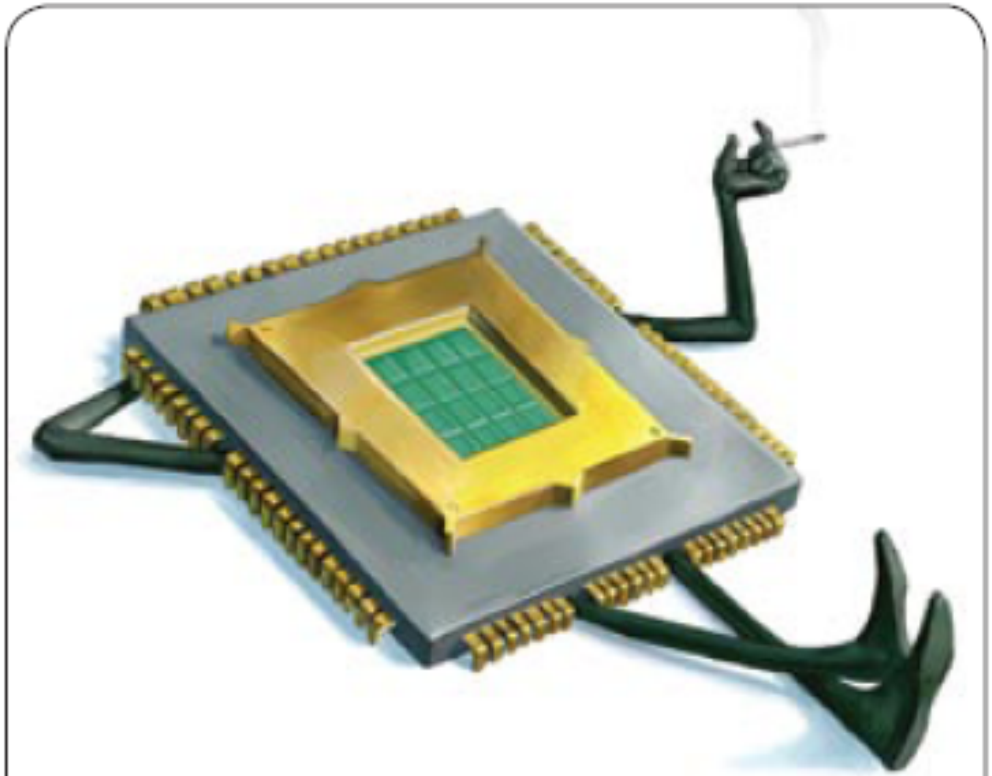
## WHO PAYS?

LOOK FOR NEW APPLICATIONS!

- CELLULAR NONLINEAR/NEURAL NETWORKS
- MAGNETIC COMPUTER
- BIO-IMPLANTED PROSTHESES

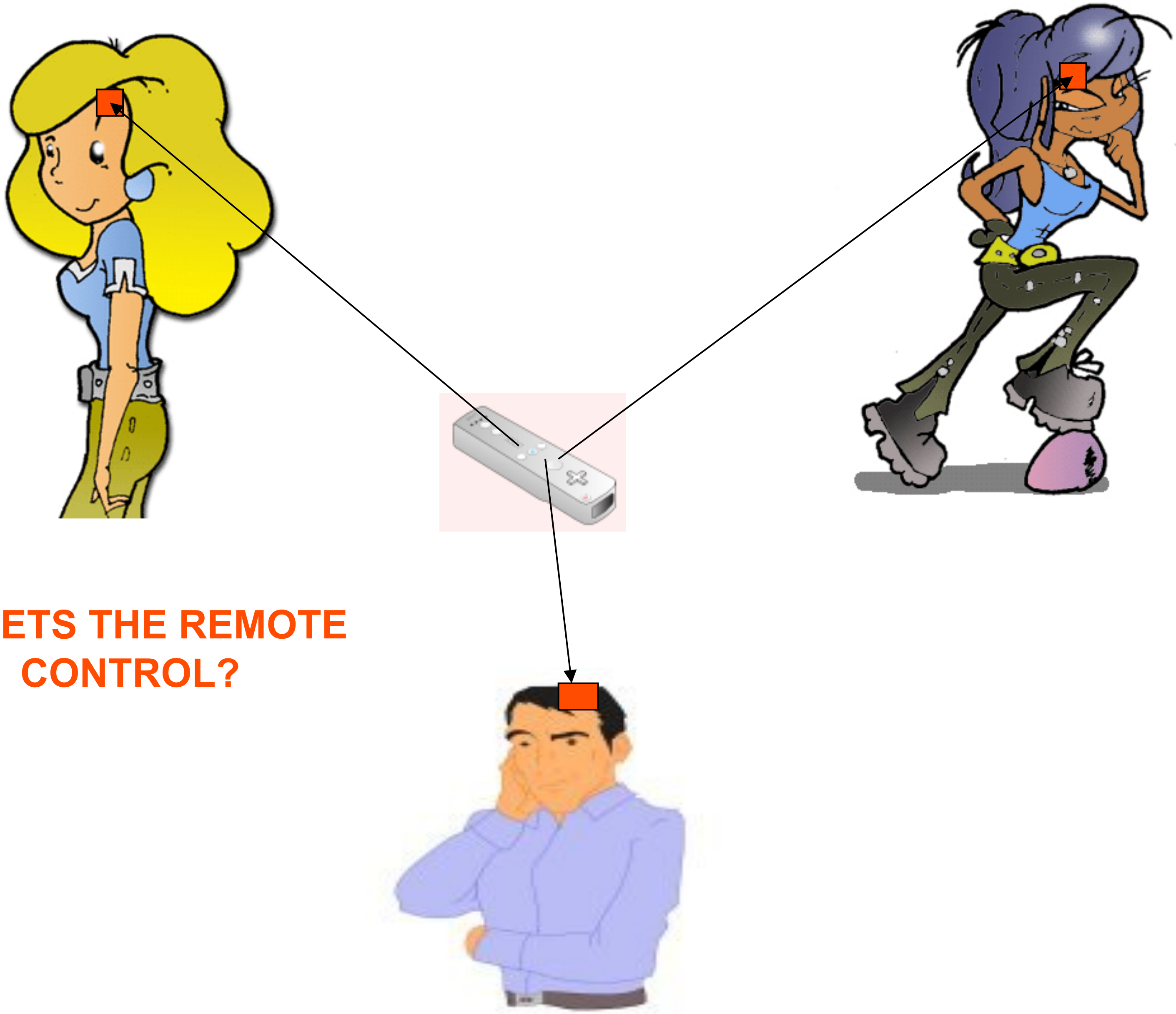
TAKE ADVANTAGE OF SPECIAL PROPERTIES OF THE NEW DEVICES

REJECT THE DEVICES WHICH DON'T MEET THE CHALLENGES



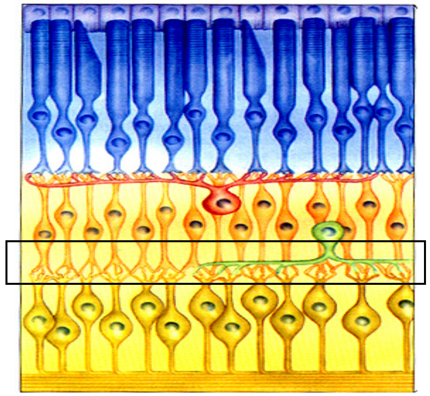
**SEX CIRCUIT:** A pleasure center in the brain may be stimulated by signals from a chip that are then sent to electrodes that zap just the right spot.

Sci. Am. May 2009

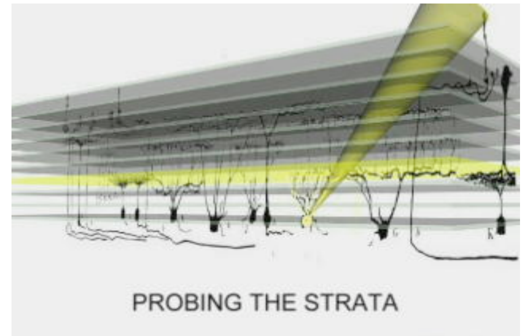


**WHO GETS THE REMOTE CONTROL?**

# Deriving the Algorithms from the Physiology

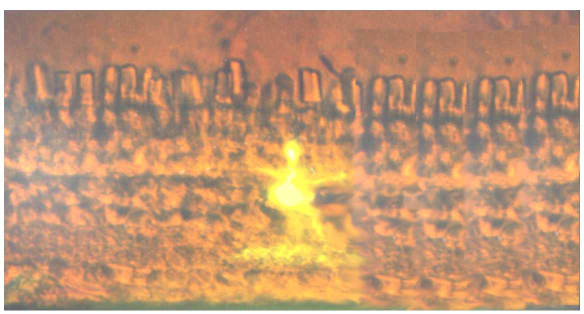


Inner Retina

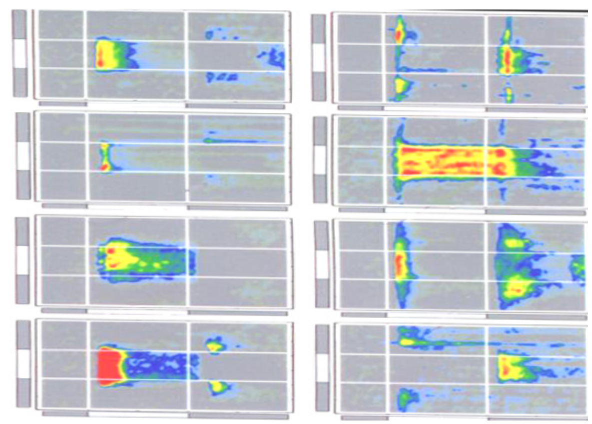



The retina is a multlayered neuronal processing center. Until recently, almost nothing was known about the processing capabilities of the inner retina shown by the box. Our studies have revealed a rich "retinal language" that extracts a variety of space-time features from the visual world.

The inner retina is comprised of more than a dozen strata.
Each stratum carries a unique representation f the visual world
These representations can be "read out" by recording electrodes



Here's an example of a living slice of retina resembling the textbook illustration above
But all cells are alive and can be studied.



This is a set of 4 of more than a dozen space-time representations derived from electrode measurements Each representation in the inner retina, is carried to the brain by a separate ganglion cell type reading from a separate stratum (above). These represent a full "feature set" of space-time filters that completely characterize the visual world for us.

# InAs/AlSb/GaSb
# The All-Purpose Electronics Material

Lattice Matched Heterojunctions

RTD and RITD-Resonant tunneling devices

- DSP (>TeraHertz)
- SRAM

Dilute Magnetic Semiconductor

Optical detector

Infra-red detectors (2-13 micron wavelengths)

TeraHertz detector for imaging systems

Low power high frequency heterojunction transistor

Nanowire transistors and diodes

Hybrid devices

Multi-value logic

Multi-state memory